

High Speed +5V Powered RS-232 Transmitters/Receivers

The HIN202A-HIN241A family of high-speed RS-232 transmitters/receivers interface circuits meet all EIA high-speed RS-232E and V.28 specifications, and are particularly suited for those applications where $\pm 12V$ is not available. They require a single +5V power supply and feature onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply. The HIN203A, HIN205A, HIN233A and HIN235A require no external capacitors and are ideally suited for applications where circuit board space is critical. The family of devices offers a wide variety of high-speed RS-232 transmitter/receiver combinations to accommodate various applications (see Selection Table).

The HIN205A, HIN206A, HIN211A, HIN213A, HIN235A, HIN236A, and HIN241A feature a low power shutdown mode to conserve energy in battery powered applications. In addition, the HIN213A provides two active receivers in shutdown mode allowing for easy "wakeup" capability.

The drivers feature true TTL/CMOS input compatibility, slew rate-limited output, and 300 Ω power-off source impedance. The receivers can handle up to $\pm 30V$ input, and have a 3k Ω to 7k Ω input impedance. The receivers also feature hysteresis to greatly improve noise rejection.

Features

- Meets All RS-232E and V.28 Specifications
- Requires Only 0.1 μF or Greater External Capacitors (HIN203A, HIN205A, HIN233A and HIN235A Require No External Capacitors)
- 230kbit/s Data Rate
- Two Receivers Active in Shutdown Mode (HIN213A)
- Requires Only Single +5V Power Supply
- Onboard Voltage Doubler/Inverter
- Low Power Consumption (Typ) 5mA
- Low Power Shutdown Function (Typ) 1 μA
- Three-State TTL/CMOS Receiver Outputs
- Multiple Drivers
 - $\pm 10V$ Output Swing for +5V Input
 - 300 Ω Power-Off Source Impedance
 - Output Current Limiting
 - TTL/CMOS Compatible
 - 30V/ μs Maximum Slew Rate
- Multiple Receivers
 - $\pm 30V$ Input Voltage Range
 - 3k Ω to 7k Ω Input Impedance
 - 0.5V Hysteresis to Improve Noise Rejection

Applications

- Any System Requiring High-Speed RS-232 Communications Port
 - Computer - Portable, Mainframe, Laptop
 - Peripheral - Printers and Terminals
 - Instrumentation, UPS
 - Modems

Selection Table

PART NUMBER	POWER SUPPLY VOLTAGE	NUMBER OF RS-232 DRIVERS	NUMBER OF RS-232 RECEIVERS	NUMBER OF 0.1 μ F EXTERNAL CAPACITORS	LOW POWER SHUTDOWN/ TTL THREE-STATE	NUMBER OF RECEIVERS ACTIVE IN SHUTDOWN
HIN202A	+5V	2	2	4 Capacitors	No/No	0
HIN203A	+5V	2	2	None	No/No	0
HIN205A	+5V	5	5	None	Yes/Yes	0
HIN206A	+5V	4	3	4 Capacitors	Yes/Yes	0
HIN207A	+5V	5	3	4 Capacitors	No/No	0
HIN208A	+5V	4	4	4 Capacitors	No/No	0
HIN211A	+5V	4	5	4 Capacitors	Yes/Yes	0
HIN213A	+5V	4	5	4 Capacitors	Yes/Yes	2
HIN232A	+5V	2	2	4 Capacitors	No/No	0
HIN233A	+5V	2	2	None	No/No	0
HIN235A	+5V	5	5	None	Yes/Yes	0
HIN236A	+5V	4	3	4 Capacitors	Yes/Yes	0
HIN237A	+5V	5	3	4 Capacitors	No/No	0
HIN238A	+5V	4	4	4 Capacitors	No/No	0
HIN241A	+5V	4	5	4 Capacitors	Yes/Yes	0

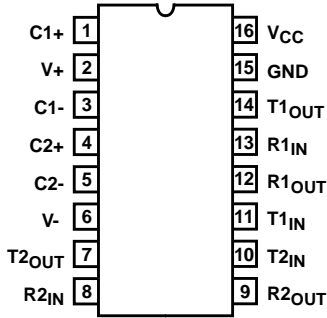
Ordering Information

PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIN202ACA-T	0 to 70	Tape and Reel	
HIN202ACB	0 to 70	16 Ld SOIC	M16.3
HIN202ACB-T	0 to 70	Tape and Reel	
HIN202ACBN	0 to 70	16 Ld SOIC	M16.15
HIN202ACBN-T	0 to 70	Tape and Reel	
HIN202ACP	0 to 70	16 Ld PDIP	E16.3
HIN203ACB	0 to 70	20 Ld SOIC	M20.3
HIN203ACB-T	0 to 70	Tape and Reel	
HIN203ACP	0 to 70	20 Ld PDIP	E20.3
HIN205ACP	0 to 70	24 Ld PDIP	E24.6
HIN206ACA	0 to 70	24 Ld SSOP	M24.209
HIN206ACA-T	0 to 70	Tape and Reel	
HIN206ACB	0 to 70	24 Ld SOIC (W)	M24.3
HIN206ACB-T	0 to 70	Tape and Reel	
HIN206ACP	0 to 70	24 Ld PDIP	E24.3
HIN207ACA	0 to 70	24 Ld SSOP	M24.209
HIN207ACA-T	0 to 70	Tape and Reel	
HIN207ACB	0 to 70	24 Ld SOIC	M24.3
HIN207ACB-T	0 to 70	Tape and Reel	
HIN207ACP	0 to 70	24 Ld PDIP	E24.3
HIN208ACA	0 to 70	24 Ld SSOP	M24.209
HIN208ACA-T	0 to 70	Tape and Reel	
HIN208ACB	0 to 70	24 Ld SOIC	M24.3
HIN208ACB-T	0 to 70	Tape and Reel	
HIN208ACP	0 to 70	24 Ld PDIP	E24.3
HIN211ACA	0 to 70	28 Ld SSOP	M28.209
HIN211ACA-T	0 to 70	Tape and Reel	
HIN211ACB	0 to 70	28 Ld SOIC	M28.3

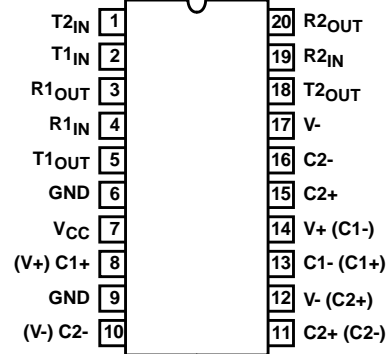
PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIN211ACB-T	0 to 70	Tape and Reel	
HIN213ACA	0 to 70	24 Ld SSOP	M28.209
HIN213ACA-T	0 to 70	Tape and Reel	
HIN213ACB	0 to 70	28 Ld SOIC	M28.3
HIN213ACB-T	0 to 70	Tape and Reel	
HIN232ACA	0 to 70	16 Ld SSOP	M16.209
HIN232ACA-T	0 to 70	Tape and Reel	
HIN232ACB	0 to 70	16 Ld SOIC	M16.3
HIN232ACB-T	0 to 70	Tape and Reel	
HIN232ACBN	0 to 70	16 Ld SOIC (N)	M16.15
HIN232ACBN-T	0 to 70	Tape and Reel	
HIN232ACP	0 to 70	16 Ld PDIP	E16.3
HIN233ACB	0 to 70	20 Ld SOIC	M20.3
HIN233ACB-T	0 to 70	Tape and Reel	
HIN233ACP	0 to 70	20 Ld PDIP	E20.3
HIN235ACP	0 to 70	24 Ld PDIP	E24.6
HIN236ACA	0 to 70	24 Ld SSOP	M24.209
HIN236ACB	0 to 70	24 Ld SOIC (W)	M24.3
HIN236ACB-T	0 to 70	Tape and Reel	
HIN236ACP	0 to 70	24 Ld PDIP	E24.3
HIN237ACA	0 to 70	24 Ld SSOP	M24.209
HIN237ACB	0 to 70	24 Ld SOIC	M24.3
HIN237ACP	0 to 70	24 Ld PDIP	E24.3
HIN238ACA	0 to 70	24 Ld SSOP	M24.209
HIN238ACB	0 to 70	24 Ld SOIC	M24.3
HIN238ACP	0 to 70	24 Ld PDIP	E24.3
HIN241ACA	0 to 70	28 Ld SSOP	M28.209
HIN241ACB	0 to 70	28 Ld SOIC	M28.3

Pinouts

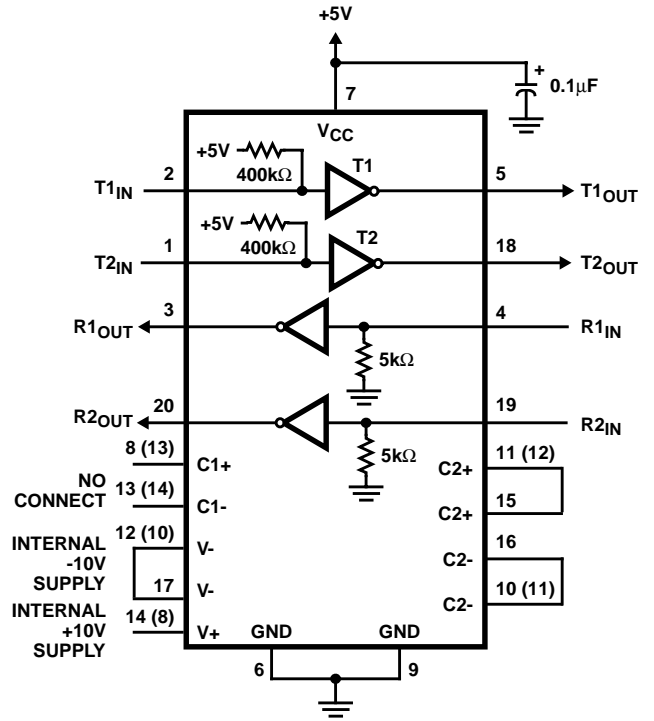
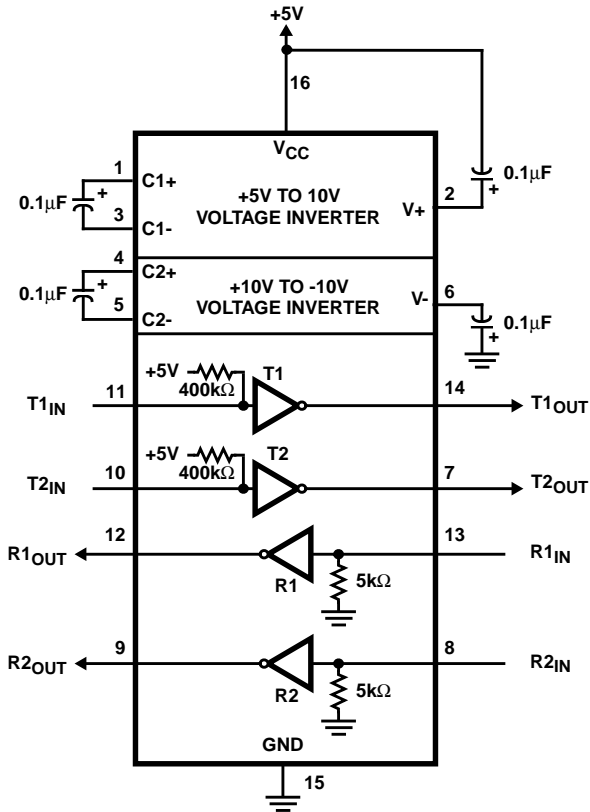
HIN202A (PDIP, SOIC)
TOP VIEW



HIN203A (PDIP, SOIC)
TOP VIEW



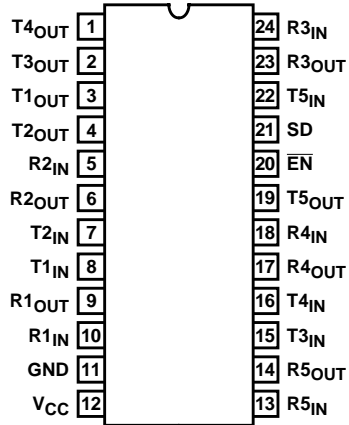
NOTE: Pin numbers in parentheses are for SOIC Package.



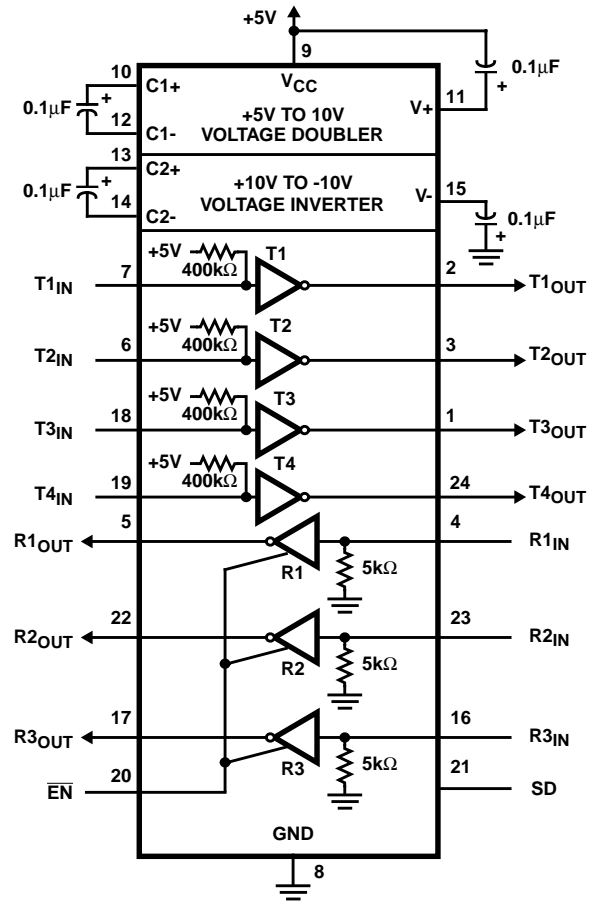
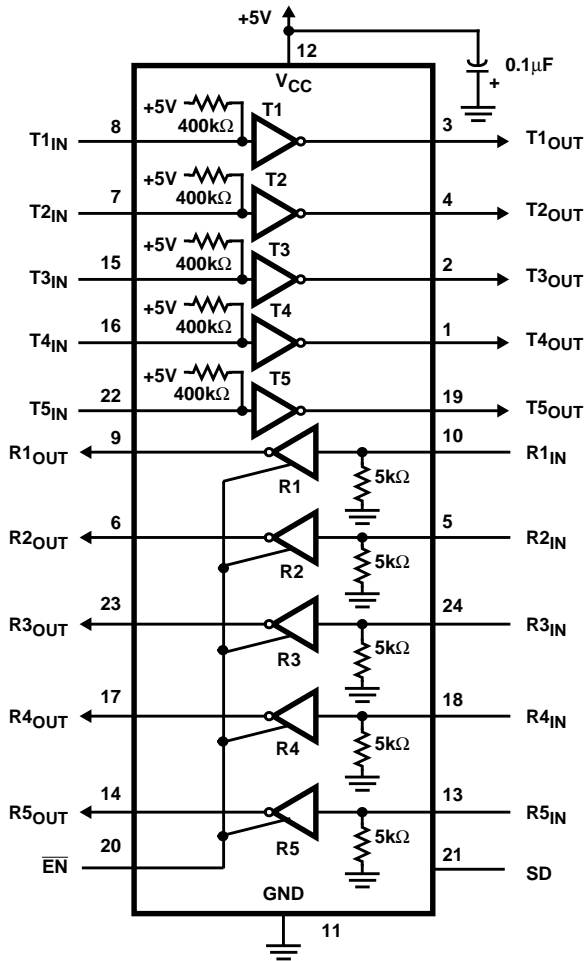
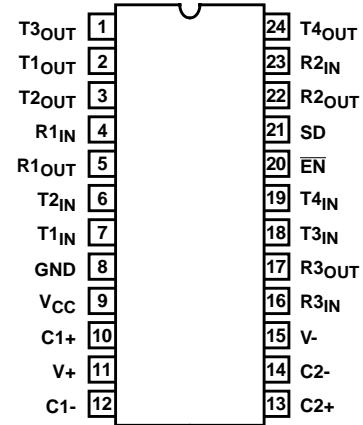
HIN202A thru HIN241A

Pinouts (Continued)

HIN205A (PDIP)
TOP VIEW

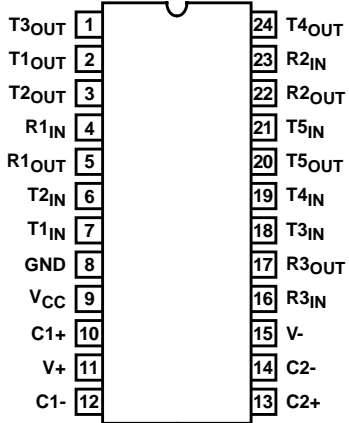


HIN206A (PDIP, SOIC, SSOP)
TOP VIEW

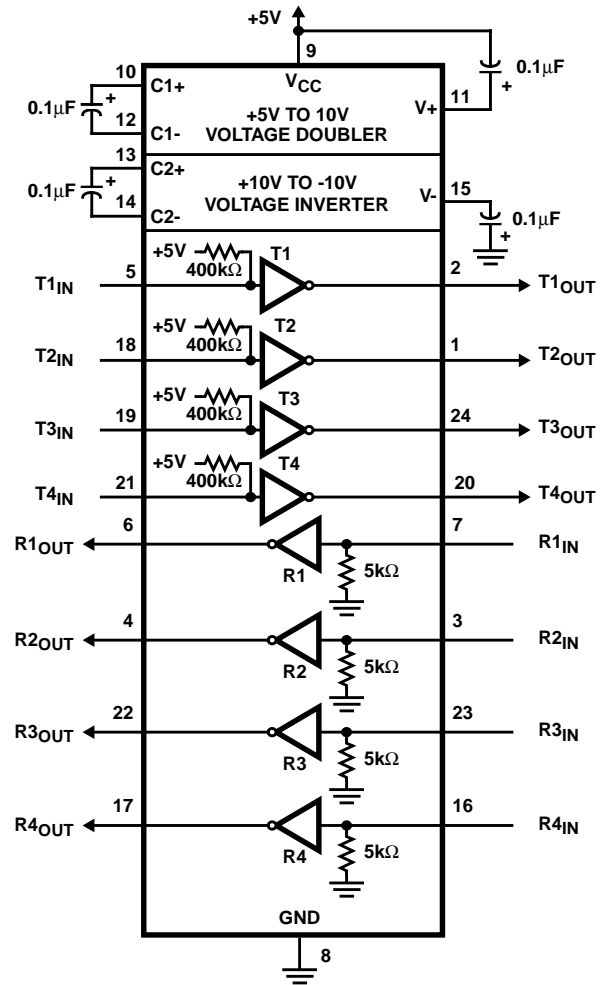
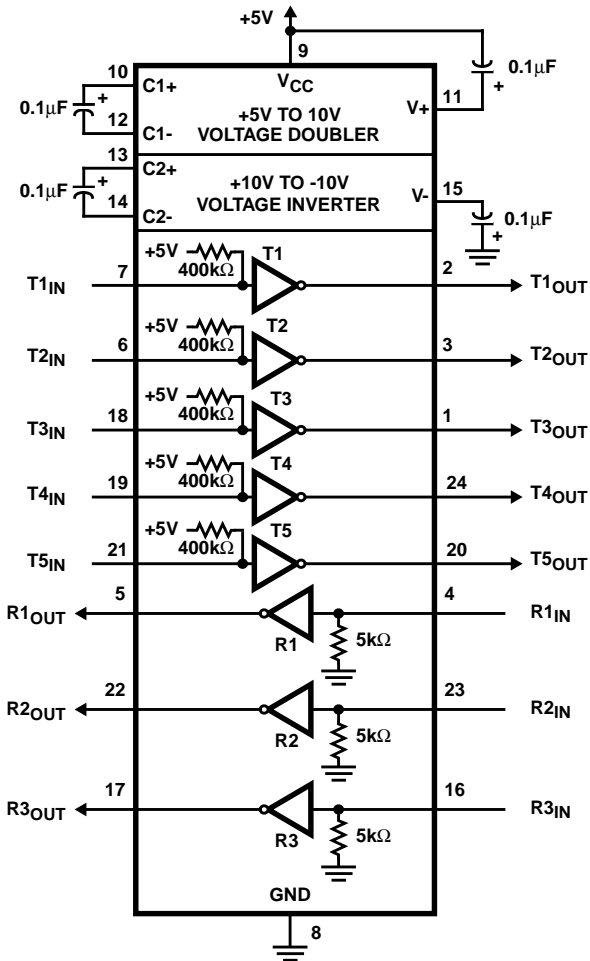
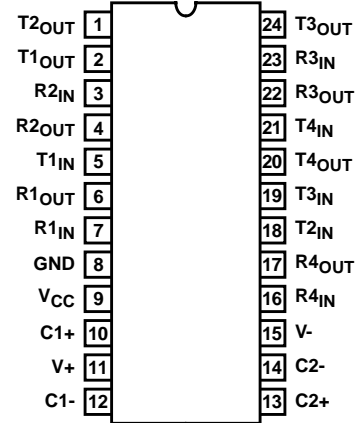


Pinouts (Continued)

HIN207A (PDIP, SOIC, SSOP)
TOP VIEW



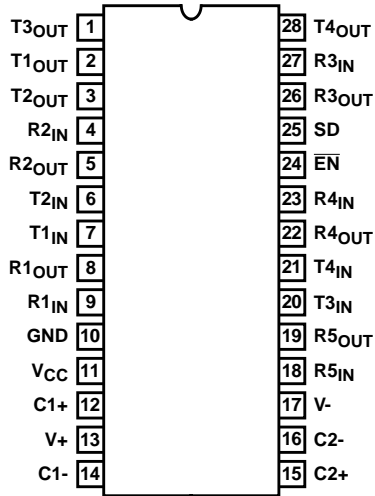
HIN208A (PDIP, SOIC, SSOP)
TOP VIEW



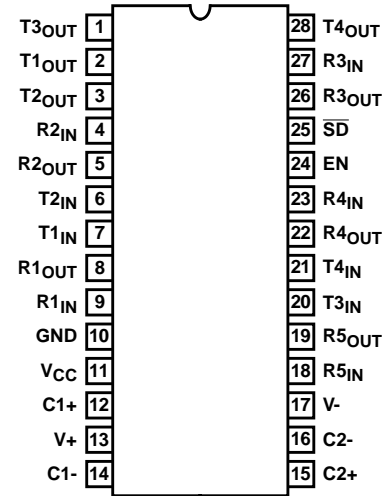
HIN202A thru HIN241A

Pinouts (Continued)

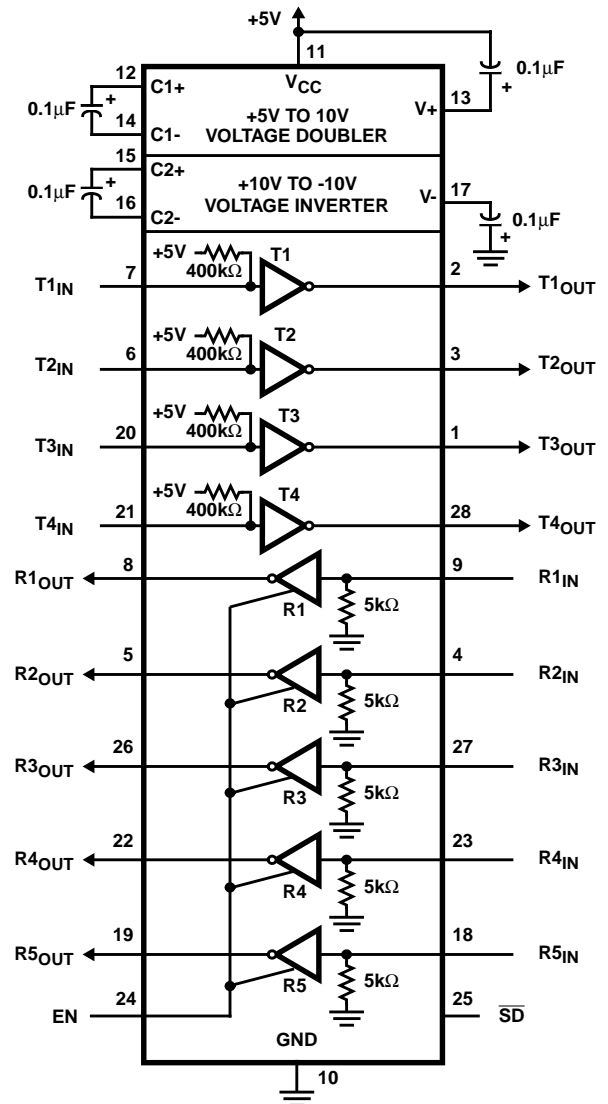
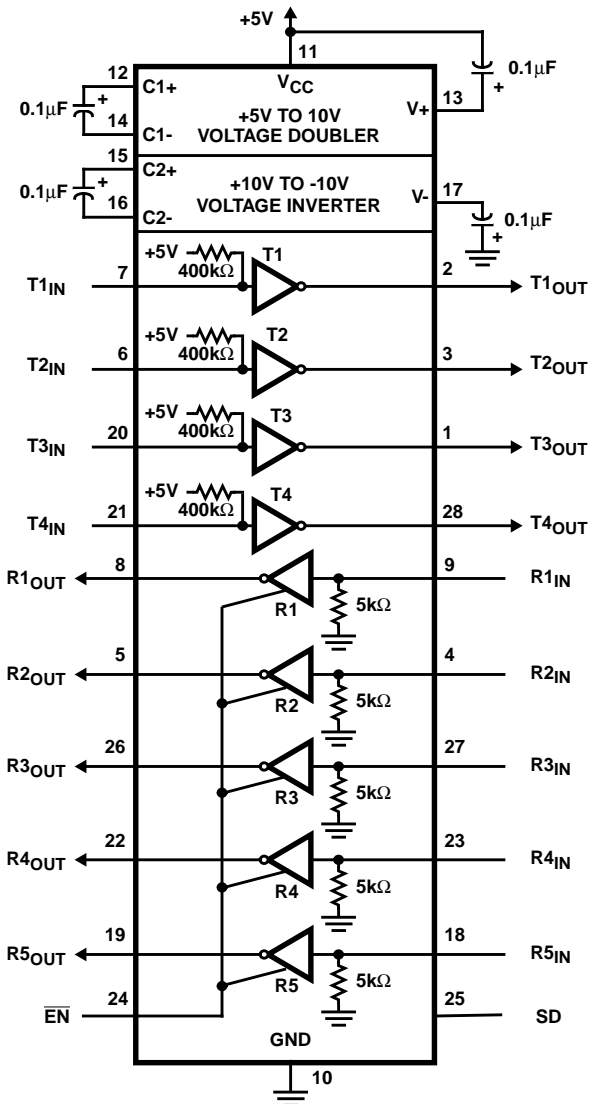
HIN211A (SOIC, SSOP)
TOP VIEW



HIN213A (SOIC, SSOP)
TOP VIEW

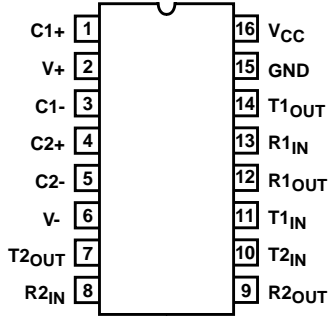


NOTE: R4 and R5 active in shutdown.

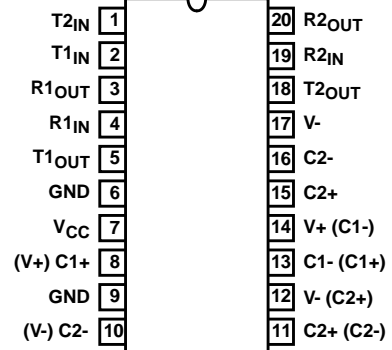


Pinouts (Continued)

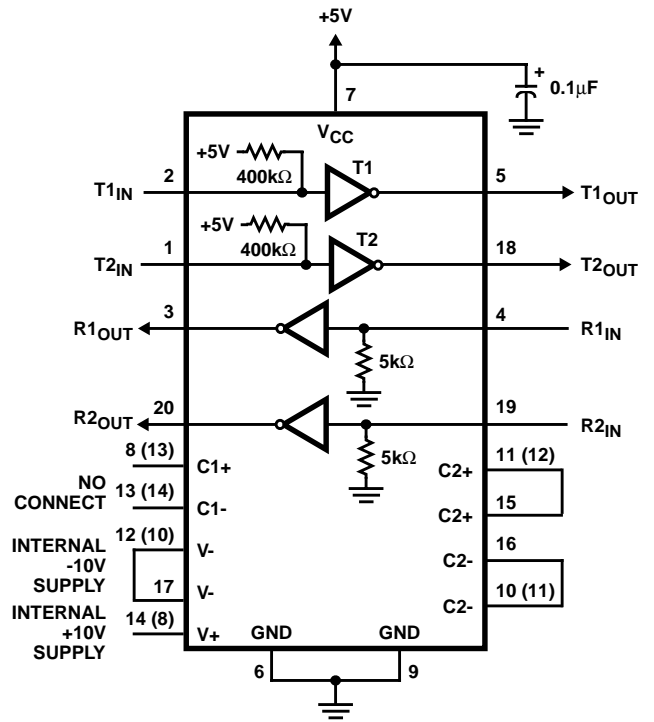
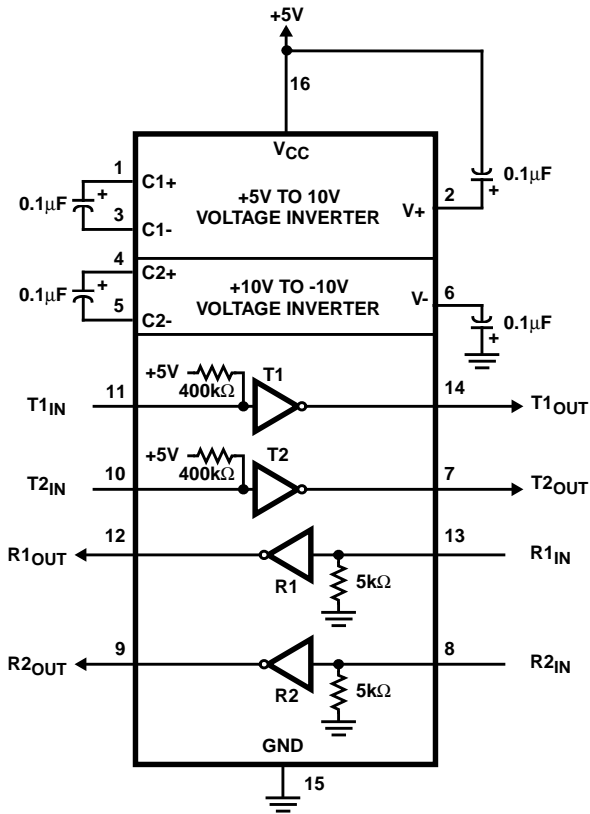
HIN232A (PDIP, SOIC)
TOP VIEW



HIN233A (PDIP, SOIC)
TOP VIEW



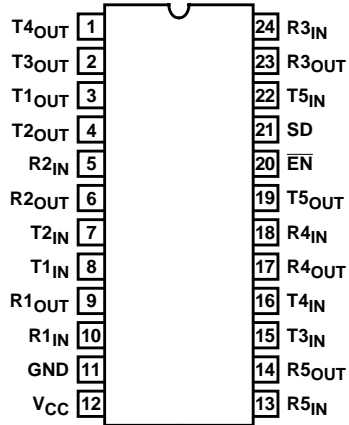
NOTE: Pin numbers in parentheses are for SOIC Package.



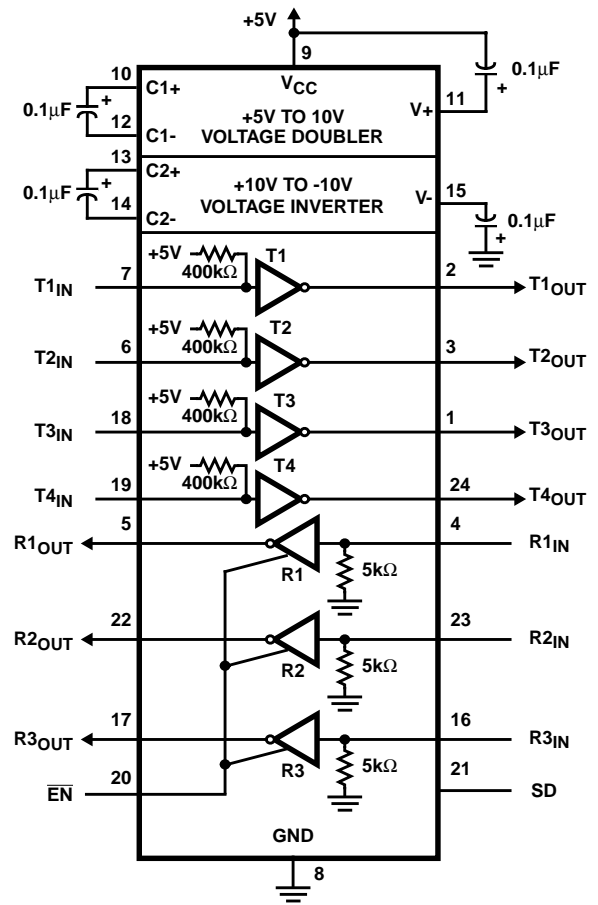
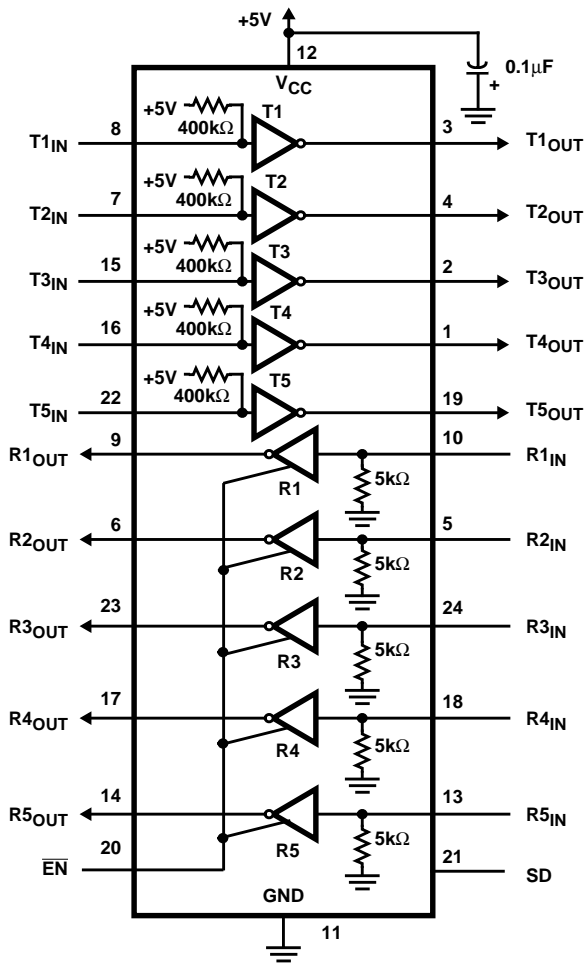
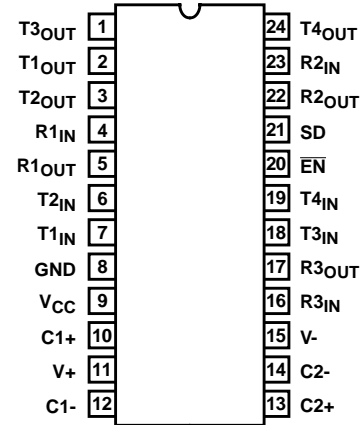
HIN202A thru HIN241A

Pinouts (Continued)

HIN235A (PDIP)
TOP VIEW

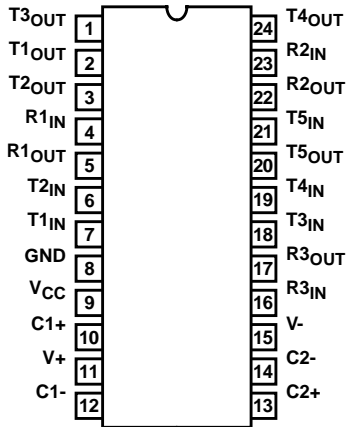


HIN236A (PDIP, SOIC, SSOP)
TOP VIEW

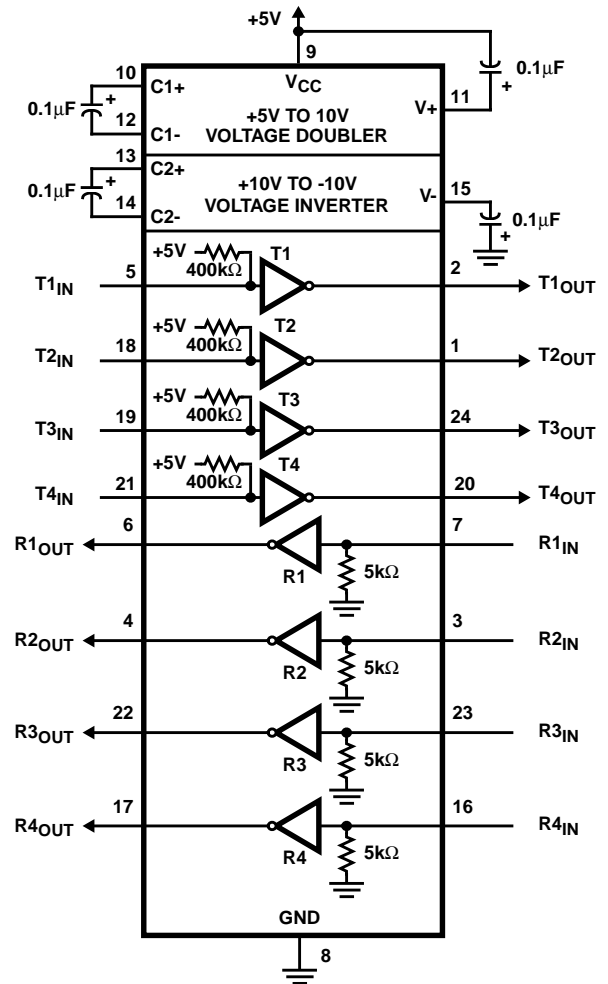
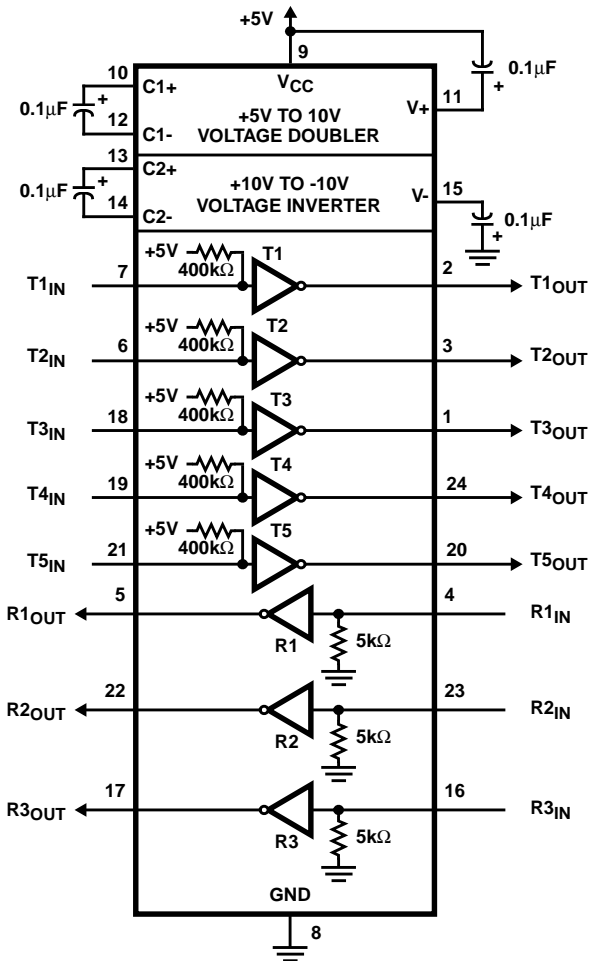
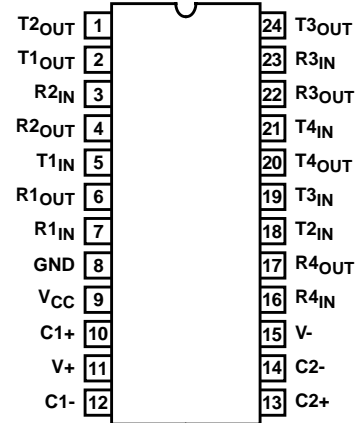


Pinouts (Continued)

HIN237A (PDIP, SOIC, SSOP)
TOP VIEW



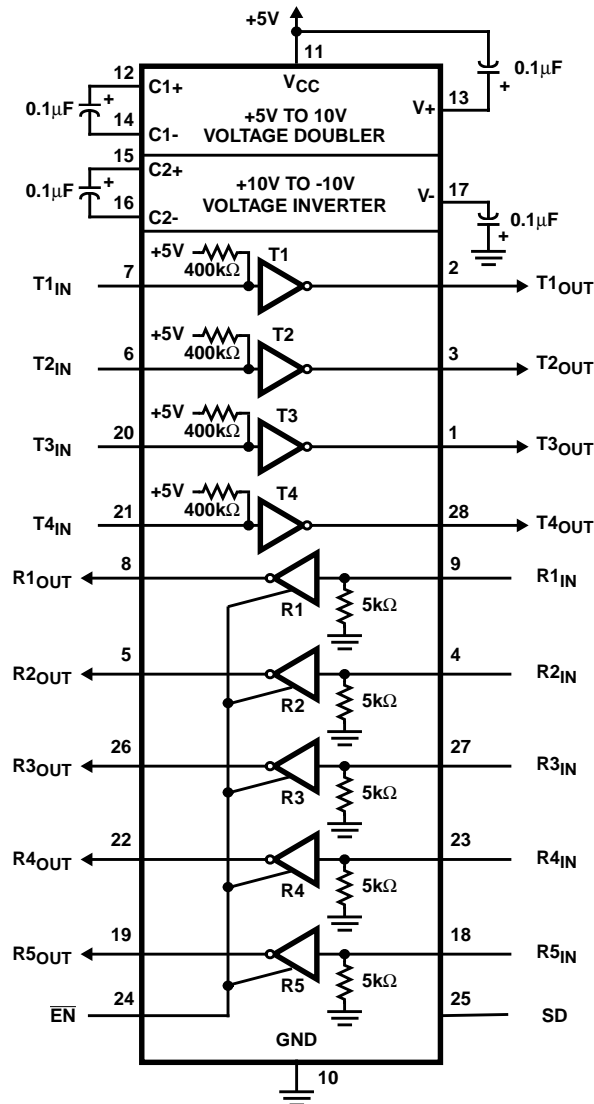
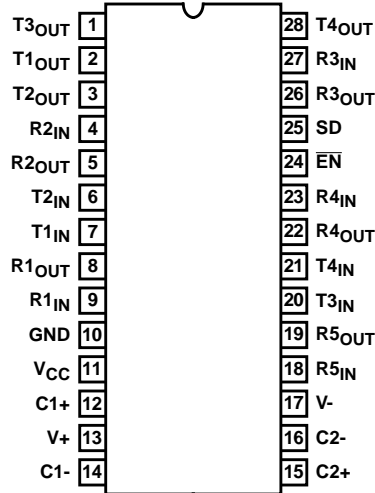
HIN238A (PDIP, SOIC, SSOP)
TOP VIEW



HIN202A thru HIN241A

Pinouts (Continued)

HIN241A (SOIC, SSOP)
TOP VIEW



Pin Descriptions

PIN	FUNCTION
V _{CC}	Power Supply Input 5V ±10%, 5V ±5% (HIN233A, HIN235A, and HIN237A).
V+	Internally generated positive supply (+10V nominal).
V-	Internally generated negative supply (-10V nominal).
GND	Ground lead. Connect to 0V.
C1+	External capacitor (+ terminal) is connected to this lead.
C1-	External capacitor (- terminal) is connected to this lead.
C2+	External capacitor (+ terminal) is connected to this lead.
C2-	External capacitor (- terminal) is connected to this lead.
T _{IN}	Transmitter Inputs. These leads accept TTL/CMOS levels. An internal 400kΩ pull-up resistor to V _{CC} is connected to each lead.
T _{OUT}	Transmitter Outputs. These are RS-232 levels (nominally ±10V).
R _{IN}	Receiver Inputs. These inputs accept RS-232 input levels. An internal 5kΩ pull-down resistor to GND is connected to each input.
R _{OUT}	Receiver Outputs. These are TTL/CMOS levels.
$\overline{\text{EN}}$	Enable input. This is an active low input which enables the receiver outputs. With $\overline{\text{EN}} = 5\text{V}$, the outputs are placed in a high impedance state.
SD, $\overline{\text{SD}}$	Shutdown Input. With SD = 5V (HIN213A $\overline{\text{SD}} = 0\text{V}$), the charge pump is disabled, the receiver outputs are in a high impedance state (except R4 and R5 of HIN241A) and the transmitters are shut off.
NC	No Connect. No connections are made to these leads.

HIN202A thru HIN241A

Absolute Maximum Ratings

V_{CC} to Ground	(GND -0.3V) < V_{CC} < 6V
V+ to Ground	(V_{CC} -0.3V) < V+ < 12V
V- to Ground	-12V < V- < (GND +0.3V)
Input Voltages	
T_{IN}	(V- -0.3V) < V_{IN} < (V+ +0.3V)
R_{IN}	$\pm 30V$
Output Voltages	
T_{OUT}	(V- -0.3V) < V_{TXOUT} < (V+ +0.3V)
R_{OUT}	(GND -0.3V) < V_{RXOUT} < (V+ +0.3V)
Short Circuit Duration	
T_{OUT}	Continuous
R_{OUT}	Continuous
ESD Classification	Class 1

Operating Conditions

Temperature Range	
HIN-XXXCX	0°C to 70°C
HIN-XXXIX	-40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
16 Ld SOIC (N) Package	115
16 Ld SOIC (W) Package	100
16 Ld SSOP Package	155
16 Ld PDIP Package	90
20 Ld SOIC Package	100
24 Ld SOIC Package	75
24 Ld SSOP Package	135
24 Ld PDIP (N) Package	75
24 Ld PDIP (W) Package	60
28 Ld SOIC Package	70
28 Ld SSOP Package	100
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(SOIC and SSOP - Lead Tips Only)	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: $V_{CC} = +5V \pm 10\%$, ($V_{CC} = +5V \pm 5\%$ HIN232A, HIN233A, HIN235A, HIN237A);
C1-C4 = 0.1 μ F; T_A = Operating Temperature Range

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing, T_{OUT}	Transmitter Outputs, 3k Ω to Ground		± 5	± 9	± 10	V
Power Supply Current, I_{CC}	No Load, $T_A = 25^\circ C$	HIN202A, HIN203A, HIN232A, HIN233A	-	8	15	mA
		HIN202A-HIN208A, HIN211A, HIN213A, HIN234A-HIN238A, HIN241A	-	11	20	mA
Shutdown Supply Current, $I_{CC}(SD)$	$T_A = 25^\circ C$	HIN205A, HIN206A, HIN211A, HIN235A, HIN236A, HIN241A	-	1	10	μ A
		HIN213A	-	15	50	μ A
Input Logic Low, T_{IN} , \overline{EN} , V_{IL}	T_{IN} , \overline{EN} , SD, EN, \overline{SD}		-	-	0.8	V
Input Logic High, V_{IH}	T_{IN}		2.0	-	-	V
	\overline{EN} , SD, EN, \overline{SD}		2.4	-	-	V
Logic Pullup Current, I_P	$T_{IN} = 0V$		-	15	200	μ A
RS-232 Input Voltage Range, V_{IN}			-30	-	+30	V
Receiver Input Impedance, R_{IN}	$T_A = 25^\circ C$, $V_{IN} = \pm 3V$		3.0	5.0	7.0	k Ω
Receiver Input Low Threshold, V_{IN} (H-L)	$V_{CC} = 5V$, $T_A = 25^\circ C$	Active Mode	-	1.2	-	V
		Shutdown Mode HIN213A R4 and R5	-	1.5	-	V
Receiver Input High Threshold, V_{IN} (L-H)	$V_{CC} = 5V$, $T_A = 25^\circ C$	Active Mode	-	1.7	2.4	V
		Shutdown Mode HIN213A R4 and R5	-	1.5	2.4	V
Receiver Input Hysteresis, V_{HYST}	$V_{CC} = 5V$ No Hysteresis in Shutdown Mode		0.2	0.5	1.0	V

HIN202A thru HIN241A

Electrical Specifications Test Conditions: $V_{CC} = +5V \pm 10\%$, ($V_{CC} = +5V \pm 5\%$ HIN232A, HIN233A, HIN235A, HIN237A); $C1-C4 = 0.1\mu F$; $T_A =$ Operating Temperature Range **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TTL/CMOS Receiver Output Voltage Low, V_{OL}	$I_{OUT} = 1.6mA$ (HIN202A, HIN203A, HIN232A, HIN233A) $I_{OUT} = 3.2mA$	-	0.1	0.4	V
TTL/CMOS Receiver Output Voltage High, V_{OH}	$I_{OUT} = -1mA$	3.5	4.6	-	V
Output Enable Time, t_{EN}	HIN205A, HIN206A, HIN211A, HIN213A, HIN235A, HIN236A, HIN241A	-	600	-	ns
Output Disable Time, t_{DIS}	HIN205A, HIN206A, HIN211A, HIN213A, HIN235A, HIN236A, HIN241A	-	200	-	ns
Transmit, Receive Propagation Delay, t_{PD}	HIN213A $\overline{SD} = 0V$, R4, R5	-	4.0	40	μs
	HIN213A $\overline{SD} = V_{CC}$, R1 - R5	-	0.5	10	μs
	All except HIN213A	-	0.5	10	μs
Transmit Transition Region Slew Rate, SR_T	$R_L = 3k\Omega$, $C_L = 1000pF$ Measured from +3V to -3V or -3V to +3V (Note 2)	3	20	45	$V/\mu s$
Output Resistance, R_{OUT}	$V_{CC} = V+ = V- = 0V$, $V_{OUT} = \pm 2V$	300	-	-	Ω
RS-232 Output Short Circuit Current, I_{SC}	T_{OUT} Shorted to GND	-	± 10	-	mA
TTL/CMOS Receiver Output Leakage	$\overline{EN} = V_{CC}$, $EN = 0$, $0V < R_{OUT} < V_{CC}$	-	0.5	± 10	μA
ESD Performance	-	-	-	-	-
ESD Protection	Human Body Model	± 15	-	-	kV
T_{IN} , R_{OUT}	IEC1000-4-2 Contact Discharge	± 8	-	-	kV
	IEC1000-4-2 Air Gap (Note 3)	± 15	-	-	kV
T_{IN} , R_{OUT}	Human Body Model	± 2	-	-	kV

NOTES:

- Guaranteed by design.
- Meets level 4 with exception of HIN205E $T5_{OUT} = \pm 12kV$.

Test Circuits (HIN232A)

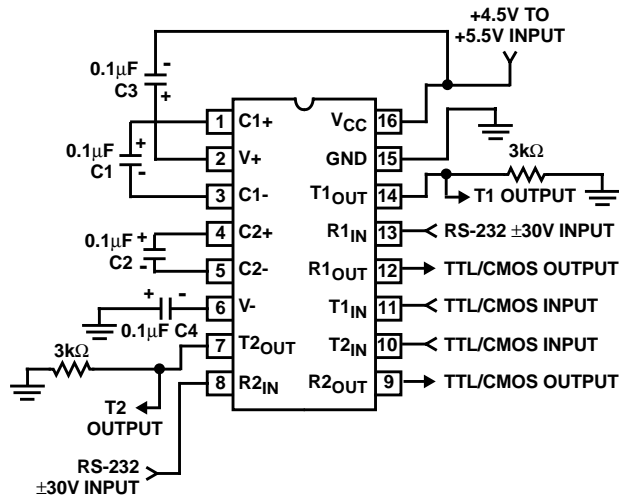


FIGURE 1. GENERAL TEST CIRCUIT

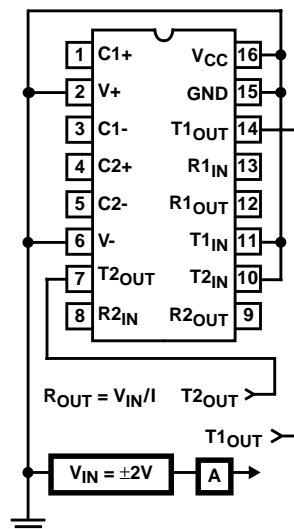


FIGURE 2. POWER-OFF SOURCE RESISTANCE CONFIGURATION

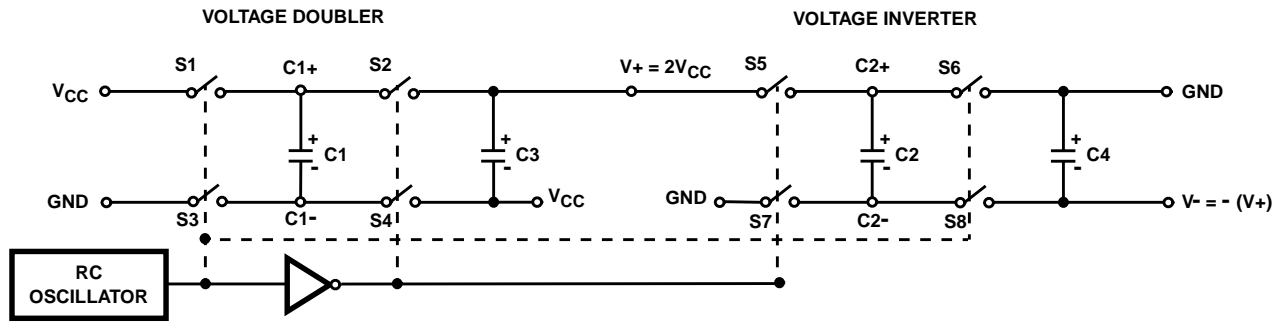


FIGURE 3. CHARGE PUMP

Detailed Description

The HIN202A thru HIN241A family of high-speed RS-232 transmitters/receivers are powered by a single +5V power supply, feature low power consumption, and meet all EIA RS232C and V.28 specifications. The circuit is divided into three sections: the charge pump, transmitter, and receiver.

Charge Pump

An equivalent circuit of the charge pump is illustrated in Figure 3. The charge pump contains two sections: the voltage doubler and the voltage inverter. Each section is driven by a two phase, internally generated clock to generate +10V and -10V. The nominal clock frequency is 125kHz. During phase one of the clock, capacitor C1 is charged to V_{CC} . During phase two, the voltage on C1 is added to V_{CC} , producing a signal across C3 equal to twice V_{CC} . During phase two, C2 is also charged to $2V_{CC}$, and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to $-2V_{CC}$. The charge pump accepts input voltages up to 5.5V. The output impedance of the voltage doubler section ($V+$) is approximately 200Ω , and the output impedance of the voltage inverter section ($V-$) is approximately 450Ω . A typical application uses $0.1\mu F$ capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the $V+$ and $V-$ supplies.

During shutdown mode (HIN202A, HIN203A, HIN205A, HIN206A, HIN211A, HIN213A, HIN232A, HIN233A, HIN235A, HIN236A and HIN241A, the charge pump is turned off, $V+$ is pulled down to V_{CC} , $V-$ is pulled up to GND, and the supply current is reduced to less than $10\mu A$. The transmitter outputs are disabled and the receiver outputs (except for HIN213A, R4 and R5) are placed in the high impedance state.

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC} , or 1.3V for $V_{CC} = 5V$. A logic

1 at the input results in a voltage of between -5V and $V-$ at the output, and a logic 0 results in a voltage between +5V and $(V+ - 0.6V)$. Each transmitter input has an internal $400k\Omega$ pullup resistor so any unused input can be left unconnected and its output voltage remains in its low state. The output voltage swing meets the RS-232C specifications of $\pm 5V$ minimum with the worst case conditions of: all transmitters driving $3k\Omega$ minimum load impedance, $V_{CC} = 4.5V$, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than $30V/\mu s$. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300Ω with $\pm 2V$ applied to the outputs and $V_{CC} = 0V$.

Receivers

The receiver inputs accept up to $\pm 30V$ while presenting the required $3k\Omega$ to $7k\Omega$ input impedance even if the power is off ($V_{CC} = 0V$). The receivers have a typical input threshold of 1.3V which is within the $\pm 3V$ limits, known as the transition region, of the RS-232 specifications. The receiver output is 0V to V_{CC} . The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis (except during shutdown) to improve noise rejection. The receiver Enable line \overline{EN} , (EN on HIN213A) when unasserted, disables the receiver outputs, placing them in the high impedance mode. The receiver outputs are also placed in the high impedance state when in shutdown mode (except HIN213A R4 and R5).

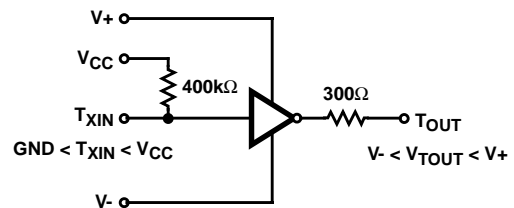


FIGURE 4. TRANSMITTER

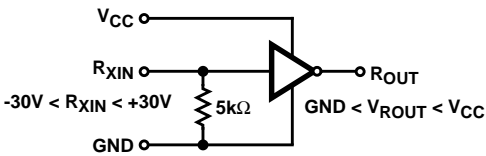
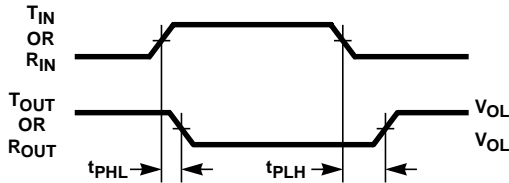


FIGURE 5. RECEIVER



$$\text{AVERAGE PROPAGATION DELAY} = \frac{t_{PHL} + t_{PLH}}{2}$$

FIGURE 6. PROPAGATION DELAY DEFINITION

HIN241A Operation in Shutdown

The HIN213A features two receivers, R4 and R5, which remain active in shutdown mode. During normal operation the receivers propagation delay is typically 0.5μs. This propagation delay may increase slightly during shutdown. When entering shut down mode, receivers R4 and R5 are not valid for 80μs after $\overline{SD} = V_{IL}$. When exiting shutdown mode, all receiver outputs will be invalid until the charge pump circuitry reaches normal operating voltage. This is typically less than 2ms when using 0.1μF capacitors.

Application Information

The HIN2XXA may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where ±12V power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 7. Fixed output signals such as DTR (data terminal ready) and DSRs (data signaling rate select) is generated by driving them through a 5kΩ resistor connected to V+.

In applications requiring four RS-232 inputs and outputs (Figure 8), note that each circuit requires two charge pump capacitors (C1 and C2) but can share common reservoir capacitors (C3 and C4). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

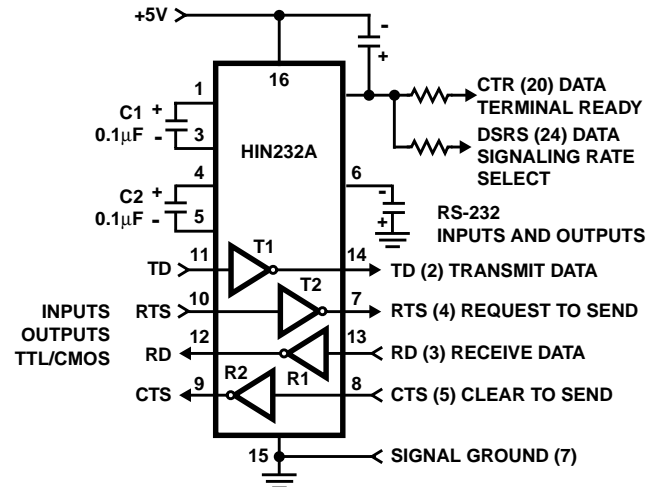


FIGURE 7. SIMPLE DUPLEX RS-232 PORT WITH CTS/RTS HANDSHAKING

HIN202A thru HIN241A

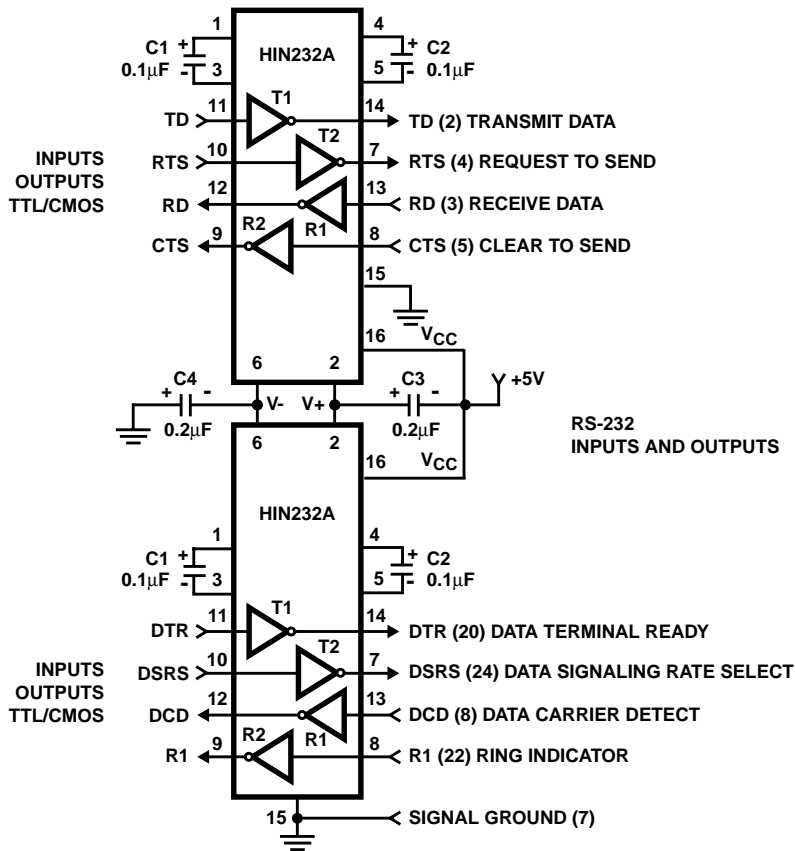


FIGURE 8. COMBINING TWO HIN232As FOR 4 PAIRS OF RS-232 INPUTS AND OUTPUTS

Typical Performance Curves

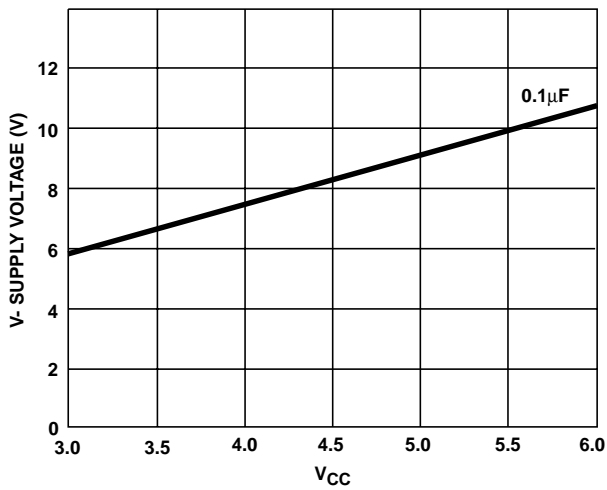


FIGURE 9. V₋ SUPPLY VOLTAGE vs V_{CC}

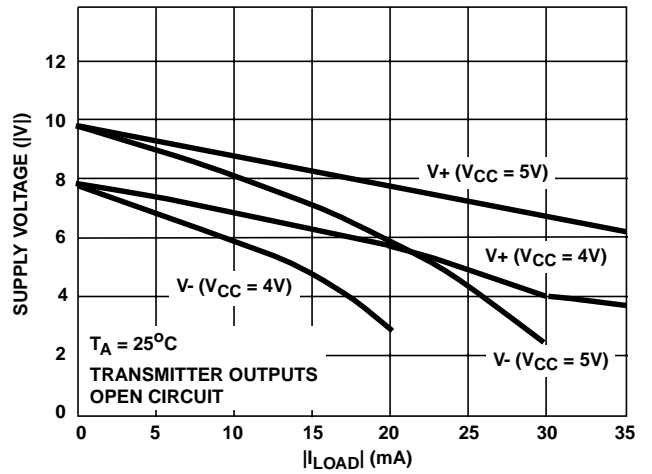


FIGURE 10. V₊, V₋ OUTPUT VOLTAGE vs LOAD

Die Characteristics

DIE DIMENSIONS:

160 mils x 140 mils

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

SUBSTRATE POTENTIAL

V+

PASSIVATION:

Type: Nitride over Silox
Nitride Thickness: 8kÅ
Silox Thickness: 7kÅ

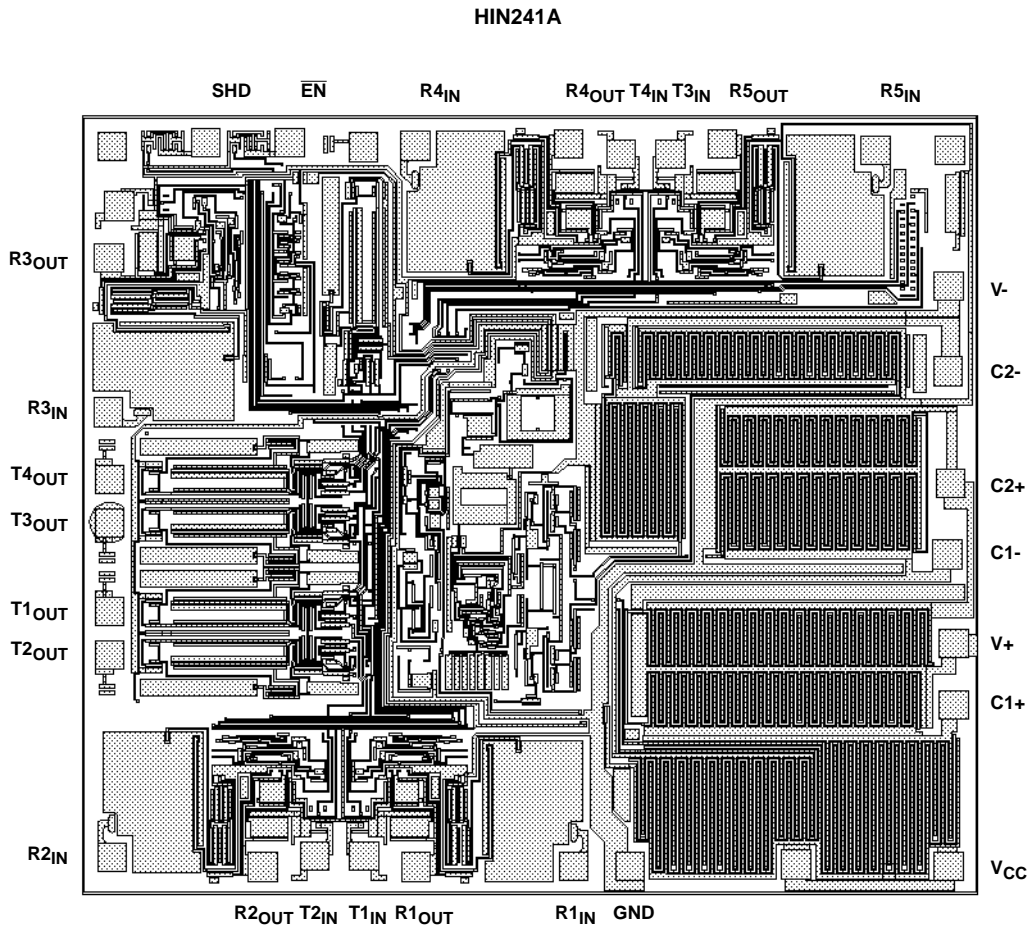
TRANSISTOR COUNT:

238

PROCESS:

CMOS Metal Gate

Metallization Mask Layout



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Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029